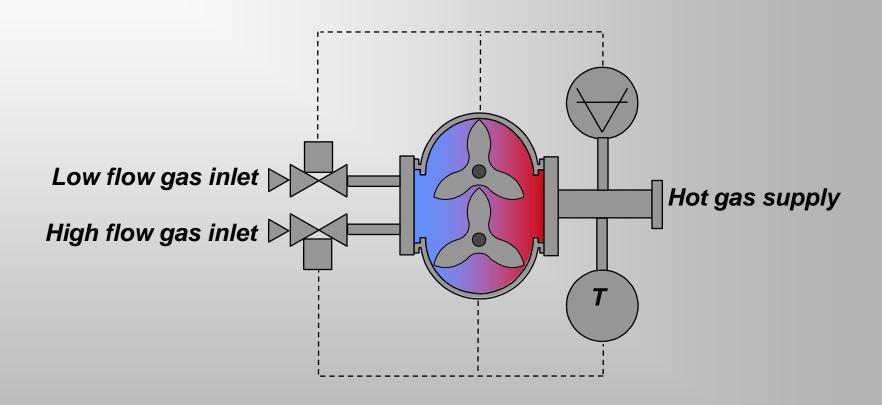
# www.Galiso.com

### **Galiso Information:**

- •Galiso was started in 1962 building equipment for high pressure testing of gas cylinders and is the number 1 supplier of this type of equipment.
- •Galiso began building equipment for Semiconductor applications in 1985. The first products that Galiso designed for this industry were automated, high purity cylinder cleaning and filling systems for semiconductor gas cylinders.
- •Galiso began building equipment to remove contamination from semiconductor vacuum process chambers in 1992. The focus of this work has been to change traditional methods for contamination removal using gas flow instead of vacuum. Galiso has received international patents on this method change.

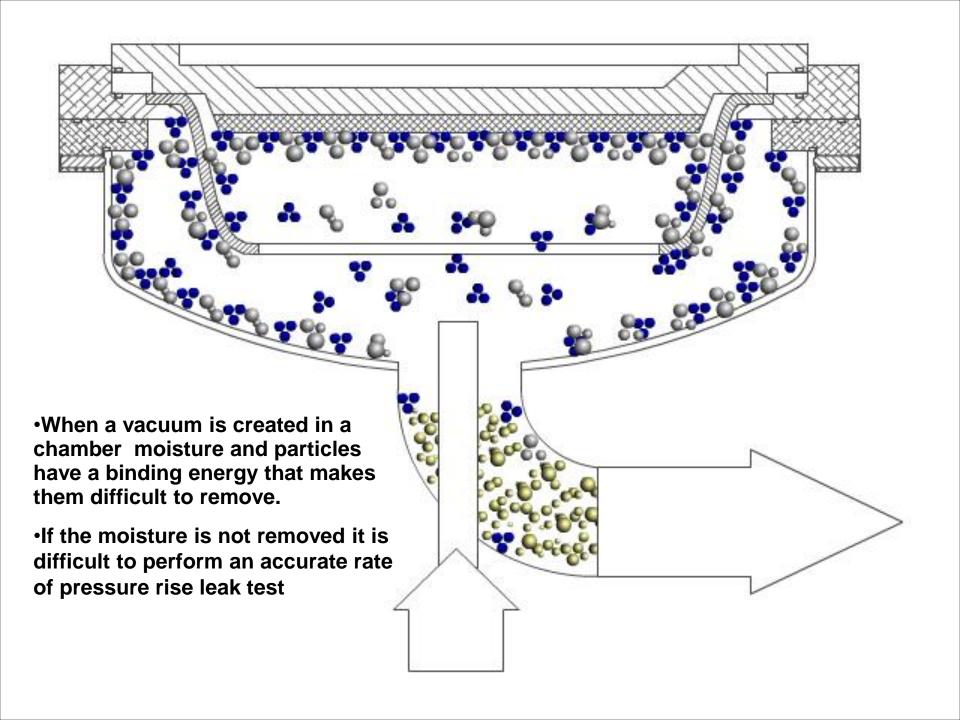


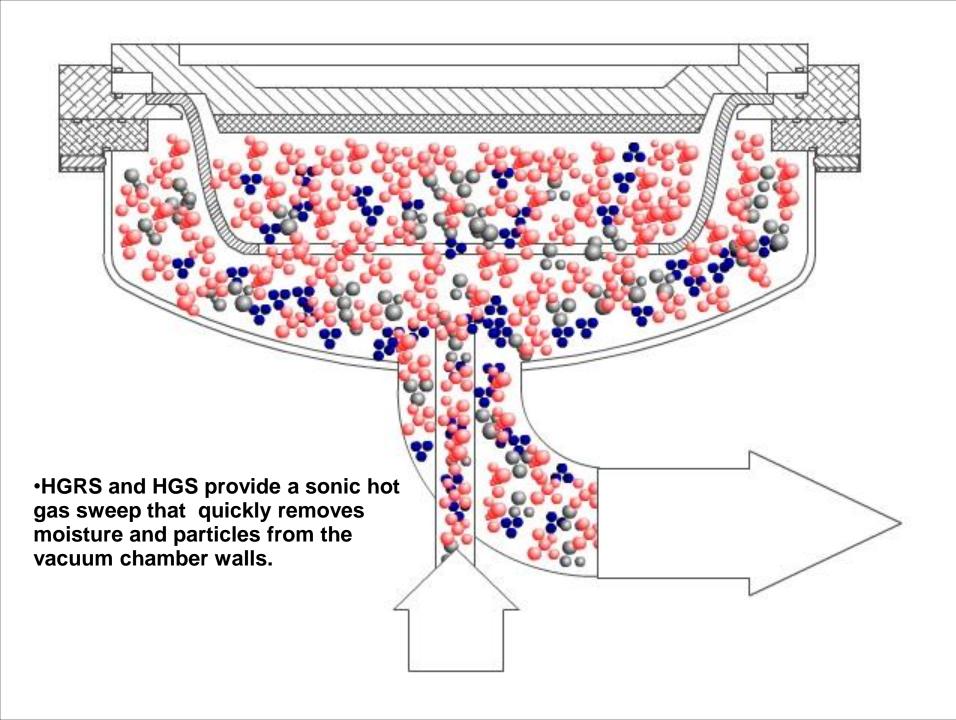


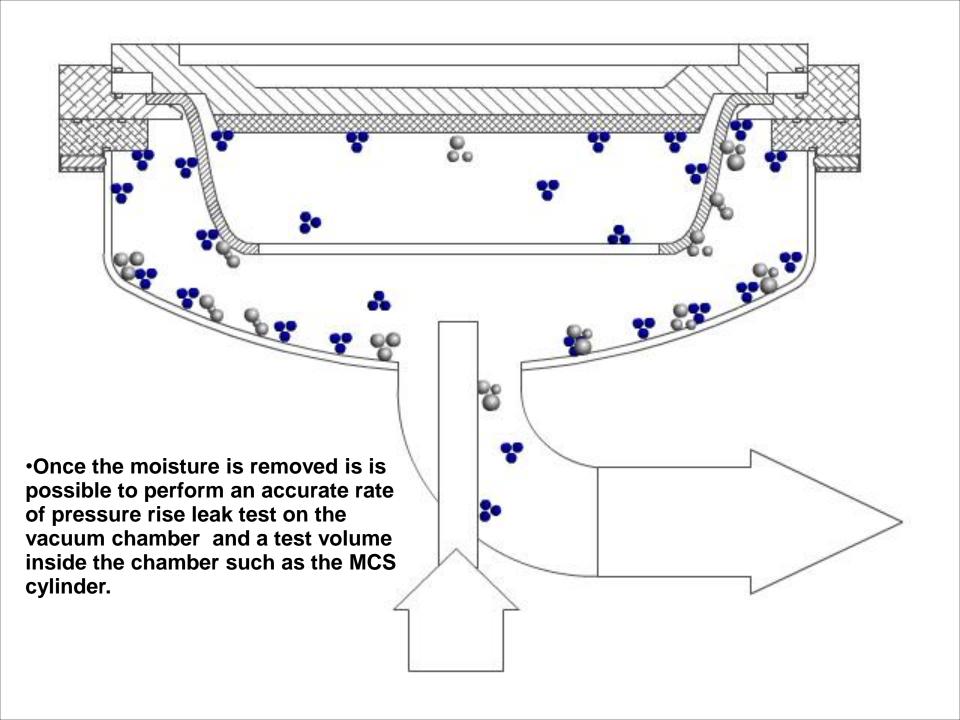


Galiso technology for contamination removal from process vacuum chambers is covered by the following patents

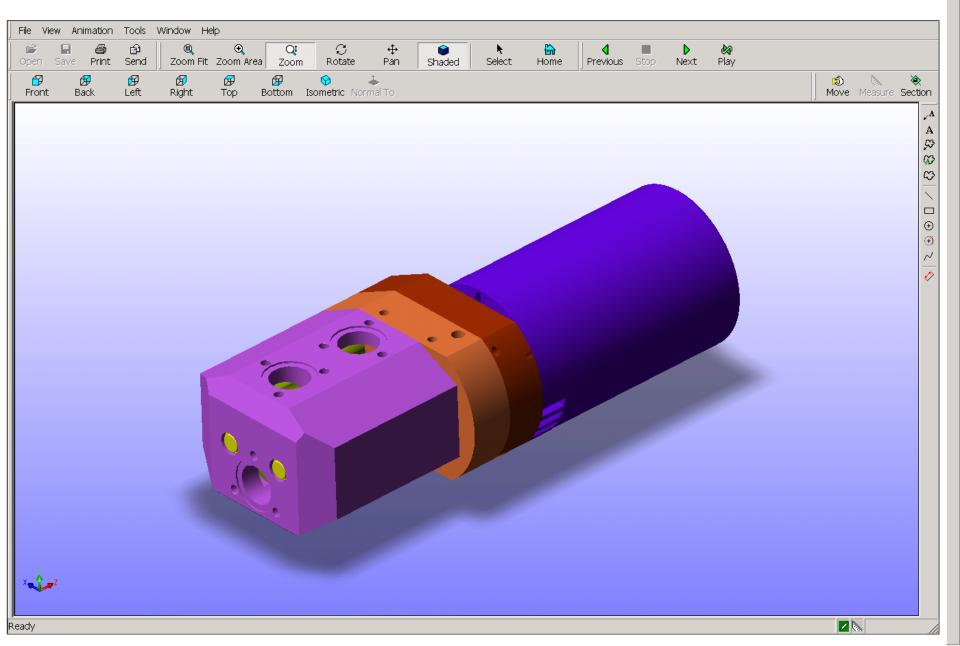
U.S.# 5,678,759 JAPAN # 2,647,266 KOREA # 166,324 U.S. AND INTERNATIONAL PATENTS PENDING







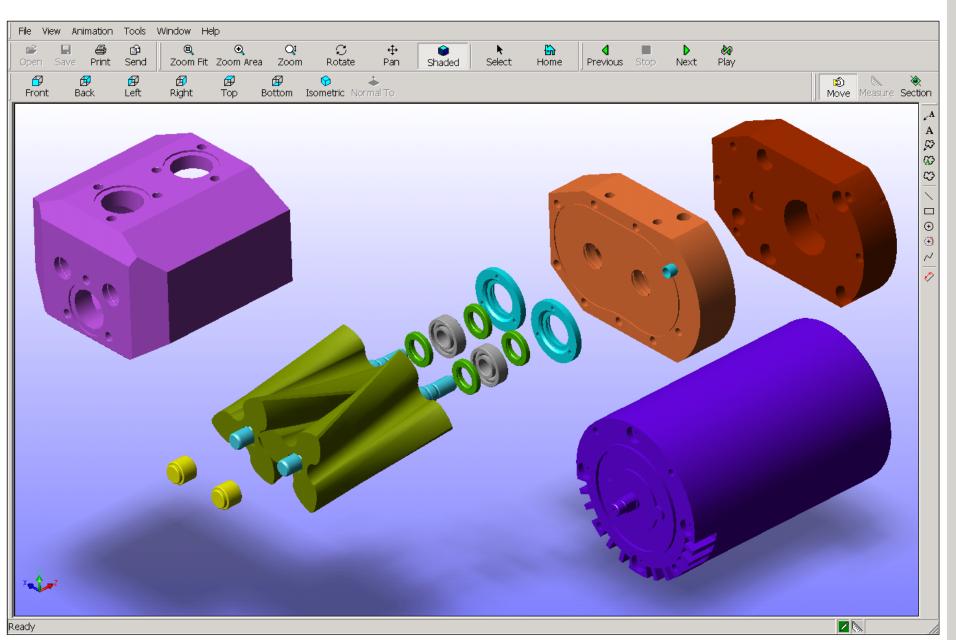
# **BLOWER ASSY1**





### <u> -</u> -

# **BLOWER ASSY1**



### **AMAT PVD Information:**

- •In 1995 Galiso used HGS technology to provide Applied Materials automated equipment for PVD chamber final test and vacuum qualification.
- •Final chamber test time was reduced from 72 hours to 24.
- •Percentage of first time chamber yield was increased from 65% to 95%



# **AMAT CVD/Etch Information:**

- In 1997 Galiso supplied Applied Materials 7 systems for automated qualification of all CVD and Etch Chambers.
- •This application reduced qualification time on etch chambers from 14 hours to 1.5 hours for DPS Poly chambers and 8 hours to 1 hour for DPS metal chambers
- •This application reduced qualification time on CVD chambers from 4 hours to 1 hours.
- •These applications were featured in AMAT manufacturing magazine.



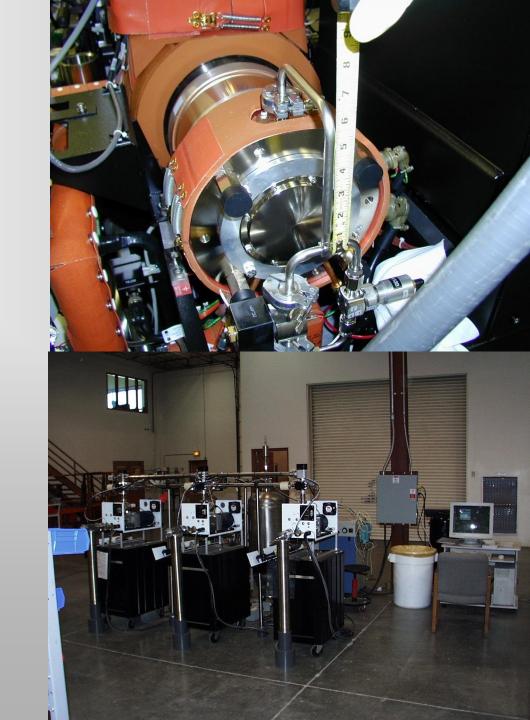
### **HGRS at Texas Instruments:**

- In 1998 Galiso demonstrated HGRS technology on Centura Tungsten etch to Texas Instruments DMOS 5
- •The result was an increase from 3000 wafers between cleans to over 14,000
- •PC tests in single digit counts during entire wafer run
- Multi Probe Yield increased 2%
- •HGS was used to reduce HBR contamination in poly etch applications at DMOS 5 centura MXP+ and K fab centura DPS



### **LAM TCP Metal Etch:**

- In 1999 Galiso demonstrated HGS technology on Lam TCP Metal Etch to Texas Instruments DMOS 5
- •The result was an increase from 1000-3000 wafers between cleans to 8000
- •PC tests in single digit counts during entire wafer run
- Multi Probe Yield increased 4%
- Automated HGS system test with He leak detector and particle counter for final test of HGS systems prior to delivery
- •In 1999 Galiso was presented a TI supplier of the year award for the performance of HGS technology at DMOS5



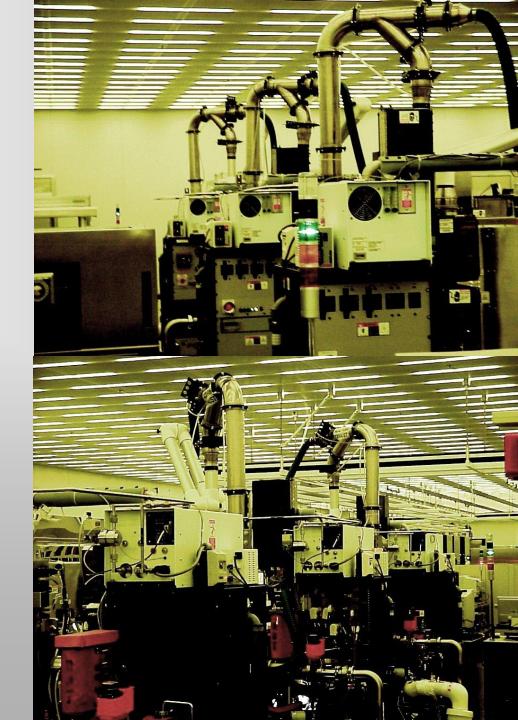
# **Cypress Semiconductor:**

- •In 2001 Galiso demonstrated HGS technology on Lam TCP Metal Etch to Cypress Semiconductor
- •The result was an increase from 150 rf hours between cleans to 400
- Product Yield increased 2%

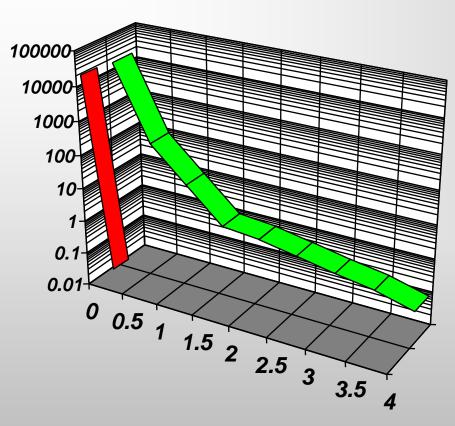


## **National Semiconductor:**

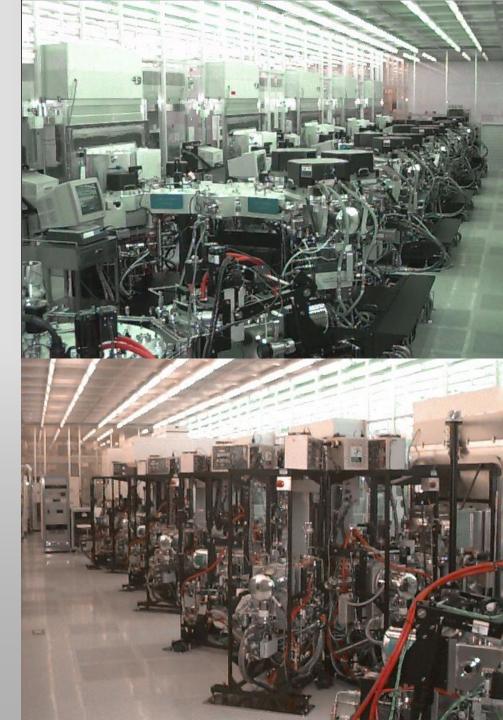
- •In 2003 Galiso demonstrated HGS technology on Lam TCP Metal Etch to National Semiconductor
- •The result was an increase from 150 rf hours between cleans to 400
- Product Yield increased 2%



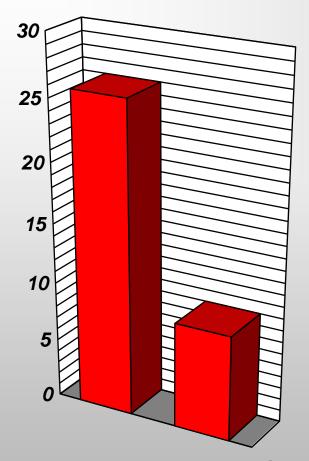
# **Intel PVD and Samsung PVD:**



•Hot Gas Recirculation and Sweep purging is able to reduce the time to achieve low ppm moisture levels. For PVD systems from Applied Materials and Varian the time was reduced from 4 hours to 30 minutes



# **Intel Scanning Electron Microscope:**



•Hot Gas Recirculation and Sweep purging is able to reduce the time to achieve high vacuum levels. For SEM systems from Hitachi the time was reduced from 24 hours to 8 hours.

